Dell™ PowerEdge™ Servers 2009 - Memory

A Dell Technical White Paper

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Executive Summary

The new R710, R610, M710, M610, T710 and T610 PowerEdge servers from Dell use the new Intel® Xeon™ 5500 series CPU that utilizes a new memory architecture. This paper discusses the new architecture, what the architecture supports, different configuration modes, and some restrictions.

Introduction

Dell servers released in early 2009 will use the new Intel® Xeon™ 5500 series CPUs that support the new DDR3 memory technology. Each CPU has three separate memory controller hubs (MCHs) within the CPU package; memory transactions no longer need to transfer between the CPU and another external device.

DDR3 memory offers some benefits over the previous FBD or DDR2 technologies; most notably higher bandwidth and lower power. There are different types of DDR3 memory supported by this platform that will be discussed later in this paper.

Finally, the inclusion of three MCHs per CPU brings some new considerations on how to best populate the system based upon the RAS features and speed.

DDR3 Memory

There are two types of DDR3 memory supported by these systems: UDIMM and RDIMM. UDIMMs are unbuffered DIMMs, while RDIMMs are registered DIMMs. The registry allows RDIMMs to potentially run at higher frequencies and support more DIMMs within a memory channel. Table 1 describes the main differences between the UDIMM and RDIMM technologies supported by Dell.

	UDIMM	RDIMM
Register/Buffer?	No	Yes
Frequencies	800, 1066, 1333MHz	800, 1066, 1333MHz
Ranks Supported	1 or 2	1, 2, or 4
Capacity per DIMM	1 or 2 GB	1, 2, 4, or 8 GB
Max # DIMMs per Channel	2	3
DRAM Technology	x8	x4 or x8
Temperature Sensor	Yes	Yes
ECC	Yes	Yes
SDDC	Yes	Yes
Address Parity	No	Yes

TABLE 1: UDIMM and RDIMM Comparison

Currently, 1 GB based DRAMs are the norm, and the table assumes 1 GB based memory; as 2 GB becomes more abundant, the noted capacities will double.

NOTE: Dell systems only support UDIMMs with ECC capabilities; UDIMMs purchased for consumer systems will typically not work in the servers.

Generally, RDIMMs should be purchased by customers who need large amounts of memory (up to 8 GB DIMMs), a broader future memory expansion roadmap (due to the ability to achieve three DIMMs per channel), and the latest RAS features (address parity). UDIMMs should be purchased by customers who need a limited amount of memory and are looking for power and cost savings. RDIMMs use about 1 W of power more per DIMM than the comparable UDIMMs due to the register feature. However, the register feature will allow for performance improvements when the memory is being highly utilized.

Memory Population

Each CPU has three integrated MCHs that have their own memory channel. Memory can be accessed across the CPUs, or the system can be configured in non-uniform memory architecture (NUMA). This can be configured via a BIOS configuration setting. Figure 1 shows the CPU and memory layout on the x710 models that supports up to 3 DIMMs per channel.

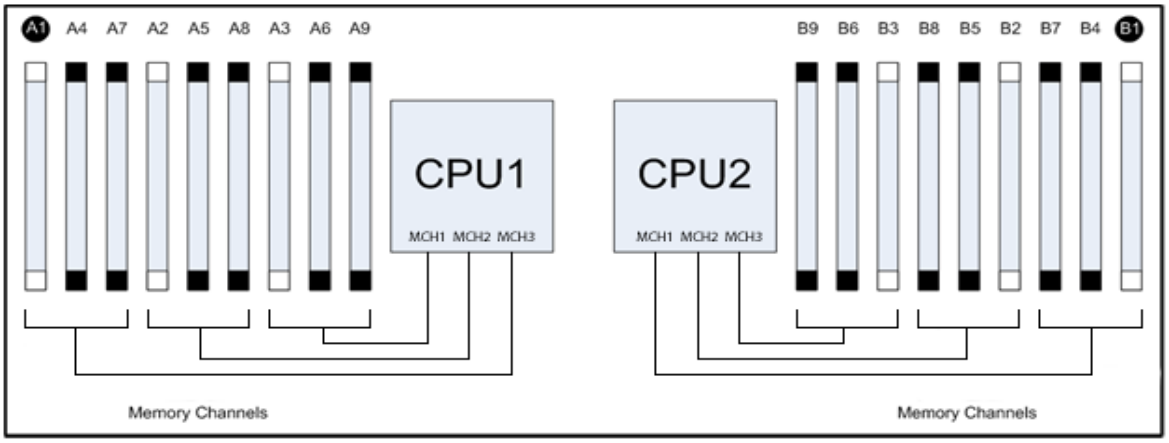

Figure 1: CPU and Memory Layout

Memory Optimized Mode

In this mode, the MCHs run independently of each other; for example, one can be idle, one can be performing a write operation, and the other can be preparing for a read operation. Memory may be installed in one, two, or three channels. To fully realize the performance benefit of the memory optimized mode, all three channels per CPU should be populated. This implies that some 'atypical' memory configurations, such as 3GB, 6GB, or 12GB, will yield the best performance. This is the recommended mode unless specific RAS features are needed.

Advanced ECC Mode

This mode uses two MCHs and "ties" them together to emulate a 128-bit data bus DIMM. This is primarily used to achieve a Single Device Data Correction (SDDC) for DIMMs based on x8 DRAM technology. SDDC is supported with x4 based DIMMs in every memory mode. One MCH is completely un-utilized, and any memory installed in this channel will generate a warning message during POST.

Mirror Mode

One of the RAS-memory modes is mirror mode. This mode uses two of the three channels. Identical data writes are performed on each channel, and reads alternate between the two channels. If excessive memory errors are detected on a channel, then that channel is disabled and the system uses the other channel for future reads and writes. This is essentially a data back-up, and allows the system to continue running even during a catastrophic DIMM failure on a channel. Since the memory is copied between DIMMs, the operating system will only see and report half of the installed memory.

Population

Table 2 shows how to populate the system memory for each of the modes, based upon the DIMMs per channel (DPC). This table is for a single CPU; on a dual-CPU system the memory configuration between the CPUs must be identical. Memory in a row with in a table cell needs to be the same capacity and architecture. For example, in 2DPC with 2 Channels used, A1 and A2 need to match, and A4 and A5 need to match, plus A1 and A4 do need to match. Do not mix any

DIMM capacities per channel. Also, at launch, one and three channel configurations will be pre-configured in Memory Optimized mode. Two channel configurations ordered from Dell will be pre-configured in either Advanced ECC or Mirror mode; the mode will be shown at each memory selection so that the correct mode is ordered.

	1 DPC	2 DPC	3 DPC (R/S/T710 Only)
Memory Optimized			
1 Channel Used	A1		
2 Channels Used	A1, A2	A1, A2 A4, A5	A1, A2 A4, A5 A7, A8
3 Channels Used	A1, A2, A3	A1, A2, A3 A4, A5, A6	A1, A2, A3 A4, A5, A6 A7, A8, A9
Advanced ECC Or Mirror			
2 Channels Used	A2, A3	A2, A3 A5, A6	A2, A3 A5, A6 A8, A9

TABLE 2: Population Rules for Memory Modes

Memory Frequency Limitations

Due to technology limitations, frequency support has some dependency on the DPC and the ranks used in a DIMM. Table 3 shows the maximum memory frequency achievable based upon DPC and the ranks (single, dual, or quad).

NOTE: One population restriction is that any quad-rank DIMM must be the first DIMM installed in a channel; other than that, the ranks may be mixed.

Be aware that this table is subject to change as Dell and Intel work with newer technologies.

DIMM 0	DIMM 1	DIMM 2	# of DIMMs	800	1066	1333
SINGLE			1			
DOUBLE			1			
QUAD			1			
SINGLE	SINGLE		2			
SINGLE	DOUBLE		2			
DOUBLE	DOUBLE		2			
QUAD	SINGLE		2			
QUAD	DOUBLE		2			
QUAD	QUAD		2			
SINGLE	SINGLE	SINGLE	3			
SINGLE	SINGLE	DOUBLE	3			
SINGLE	DOUBLE	DOUBLE	3			

DOUBLE	DOUBLE	DOUBLE	3			
				Supported		
				Not Supported		

TABLE 3: Speed and Population Dependencies

Memory Selection

With all of these new choices, there are some questions around how to best configure a system. While each user's needs differ, there are some general guidelines around highest performance and high capacity.

High Performance

For a design which maximizes bandwidth, use DDR3 1333MHz memory across all three channels per CPU. Due to the frequency limitations shown above, this speed can only support 1 DIMM per channel, and thus a maximum of 3 DIMMs/CPU. Also, no quad-rank DIMMs may be used. At time of launch, dual rank 4GB RDIMMs provide the highest capacity at 1333MHz and will provide 12GB/CPU system capacity. Be aware that RDIMMs will provide a higher throughput during heavy utilization than UDIMMs.

Balanced Performance

The system should still be populated with DIMMs across all three channels, but 1066MHz DIMMs may be used and can be populated with two DIMMs per channel. 48GB/CPU may be achieved by installing dual-rank 8GB 1066MHz RDIMMs.

High Capacity

At the time of launch 8GB RDIMMs are the highest capacity being offered. By using the dual-rank 8GB 1066MHz RDIMMs, 72GB/CPU system capacity may be achieved. Note that since each memory channel will have 3 DIMMs installed, the system will automatically down-clock itself to 800MHz. We do not expect 800MHz based RDIMMs to be readily available during or after launch.

Mirror Mode or Advanced ECC

If SDDC support for x8 memory or mirroring is desired, then only two channels from each CPU should be populated. The memory channel farthest from the CPU should not have any DIMMs installed (A1, A4, A7, B1, B4, & B7 should remain empty), and it is vital that the DIMMs across the channels match each other as described in the Population section.

Power Conscious

UDIMMs will use less power than RDIMMs and offer fairly comparable performance to RDIMMs. However, at launch, UDIMMs are limited to a maximum 2GB capacity, and as previously described cannot support 3 DIMMs per channel. A 1066MHz configuration will use less power than one set up as 1333MHz.